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Design of Systolic Array Multiplier Circuit using Reversible Logic

Debashish Mahapatra[1], Kinnera Vishal[2], Adi Manindra[3], Bandapally Deepak[4], B Nagavardhan[5]

Department of ECE, GITAM University, Hyderabad, India[1-5]

Abstract: For data transmission, an ideal communication relies on Low Power Design. Systolic array multiplier with the reversible logic is widely known among those techniques for synchronizing signals in DSP processor applications. Low power circuit design yields many favorable conditions like increased performance, system capacity, minimized cost etc. Reversible logic is a phenomenal approach to reduce heat dissipation and information loss. Among basic arithmetic operations, Multiplication demands more processing time and seek complex hardware. As Conventional Systolic Array Multiplier is designed using irreversible logic gates, there is undesired power dissipation. So, to improvise this downside, this paper illuminates the design of low power Systolic Array Multiplier using reversible logic gates which performs data processing in Parallelism manner [5]. Power, delay, garbage outputs and quantum cost is calculated mathematically in this paper. Finally, Cadence Virtuoso is used to obtain simulation results. 25mW is the power for the proposed design when the power of individual components is added theoretically. The overall power of the circuit is 14 μW.

Keywords: Garbage Outputs (GO), Quantum Cost (QC), Multiplier cell(MC), Peres Full Adder (PFA), Peres gate (PG), Toffoli gate(TG).

I. INTRODUCTION

Parallel array multipliers are used to achieve low power and high speed. Multipliers are devolved to meet the needs in various DSP systems. The basic principle behind multiplier is multiplication in algorithmic and structural levels. DSP applications are mainly designed with low power dissipation Multipliers [4]. Systolic algorithm is linear sequence of channels, sometimes in multi-dimension. The Systolic Array is the linear arrangement of the blocks or units like the pipelining processing. It is a homogeneous network. Each block in the arrangement computes a partial result from the inputs given to it from top of the array and the result is stored within itself. Later, the stored result is passed to the adjacent blocks down the array in the arrangement. The blocks in the design are usually similar and fixed. The operations at each stage in the arrangement are done simultaneously, which increases the speed and reduces the processing time without compromising on the results. They are used to perform correlation, matrix multiplication, data sorting tasks and convolution. In this paper a 4-bit systolic array multiplier using reversible logic is designed and implemented. In systolic array multiplication, the multiplicand and the multiplier are linearly arranged like in an array and each bit of both multiplier is multiplied with the multiplicand to obtain partial products. The carry is generated from the column. The final output is obtained by adding the partial products and carry.

Landauer states that while transmitting data certain amount of energy is dissipated for each bit lost. The formula for calculating the energy dissipated for loss of each bit is KT*log2 where T is absolute temperature and K is Boltzmann's constant.

Later, Charles Bennett [2,3] concluded that heat dissipation in a digital circuit can be minimized or eliminated by performing all the computations based on reversible logic. A circuit is reversible if we can trace back inputs from outputs and if there is one-to-one mapping between inputs and outputs. The system can run both forward and backward. The inputs are obtained from the outputs by doing the same operations backwards. So, it gives an opportunity to go to any point in the computation history. It also improves the overall performance of the circuitry by allowing higher densities and higher speeds by reducing power dissipation. In this paper the design flow of Systolic Array Multiplier circuit is explained and it is divided into three sections. Existing work is discussed in Section II. The proposed design is given in Section III. In section IV, every circuit's simulation results are shown. The mathematical calculations for Systolic Array Multiplier is given in Section V. Conclusion is given in section VI.

II. EXISTING WORK

In the existing paper [4], Systolic Array Multiplier circuit is implemented using conventional irreversible logic gates. To perform multiplication of bits by consuming the low power, the circuit is developed with reversible logic gates. This multiplication process is enhanced by Pipelining process and involves data transmission in high Parallelism. The

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multiplier involves minimum 4 stages which are required to implement 4*4 systolic array multiplier. Reversible circuits store the bits rather than throwing them away. The bits which are not computed are used to trace back the inputs from outputs. For the proposed design in this paper, the parameters like power and delay, quantum cost, number of gates, garbage outputs based on the definitions given in [1].

III. PROPOSED DESIGN FOR REVERSIBLE SYSTOLIC

This paper presents the intensified power optimized Systolic Array Multiplier using reversible logic for Multiplication of Multiple data bits. This paper designed with four multiple stages. Mainly the three stages carry's were traversed from one stage to another stage, whereas the final stage carry's are traversed by side by side blocks. The sections that follow explain the design of each circuit. The detailed design of logic cell of toffoli is given in section 3.1. The detailed design of reversible logic cell of peres full adder is given in section 3.2. In section 3.3, the detailed design of Multiplier cell is given.

3.1 Design of Toffoli Logic Cell

To develop this cell, One Xor, one buffer, two And gates are used. The garbage outputs are minimum. The quantum cost is also less which succeeds in optimising the power. It has 3 inputs and 1 output. The 4 inputs are data bits. The output is 1-bit code. Fig.1 shows the architecture of Toffoli gate.

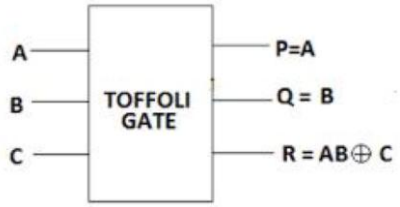

Fig. 1 Toffoli Gate

3.2 Design of Peres Full Adder Reversible Logic Cell

To develop this cell two Peres gates are used. Output of Peres Full Adder is used in Multiplier cell in section 3.3. It contains 2 outputs and 4 inputs. The main outputs are "one bit sum" and "one bit carry" and two garbage output bits Fig.2 shows detail architecture of Peres Full Adder Reversible Logic cell.

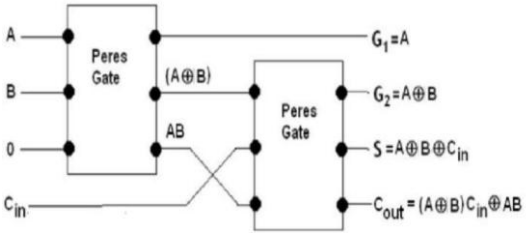

Fig. 2 Peres Gate Full Adder

3.3 Proposed the Multiplier cell block with Reversible Logic Cell

To achieve our proposed circuit, the cascading takes place in between Toffoli and Peres Full adder cells. It has two Toffoli gates and 1 Peres Full Adder gate Fig. 3 explains detail schematic of Multiplier cell block.

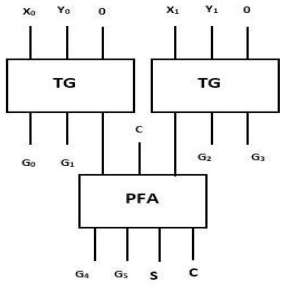

Fig. 3 Multiplier Cell Internal Architecture

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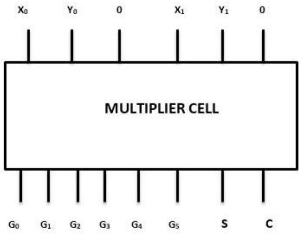

Fig. 4 Multiplier Cell Block

3.3 Proposed Systolic array multiplier using Reversible Logic Cells

To design this Multiplier, it requires four multiplier cells, Nine Toffoli Gates, Twelve Peres Full Adder are used in this paper, which succeeds in optimizing power by keeping the quantum cost as low as possible and eliminating garbage outputs. It has 8 inputs and 8 outputs. The 8 inputs are data bits. The output is 7 bits of Sum and 1 bit of Carry. The architecture of Systolic array multiplier with Reversible logic is given below S0 to S7 – Sum bits, C-Carry bit

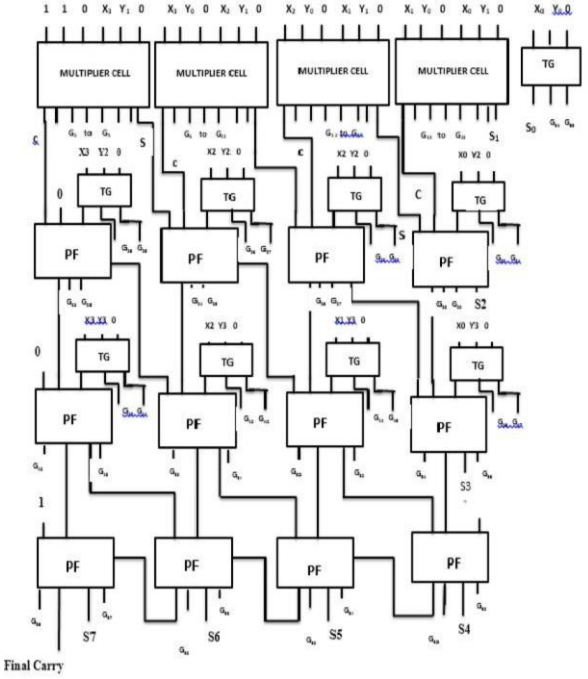

Fig.5 Systolic Array Multiplier with Reversible Logic

IV. SIMULATION RESULTS

The simulation results and power curves of each reversible logic cell used in this circuitry are depicted in this section. Simulation designs are obtained by cadence virtuoso.

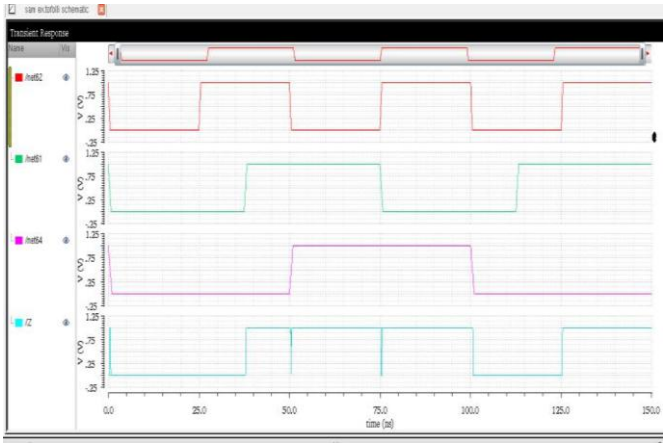

Fig. 6 Reversible Toffoli Gate simulation

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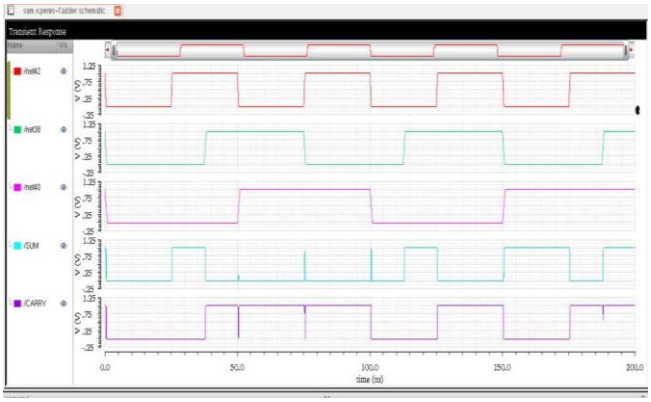

Fig. 7 Peres full adder simulation

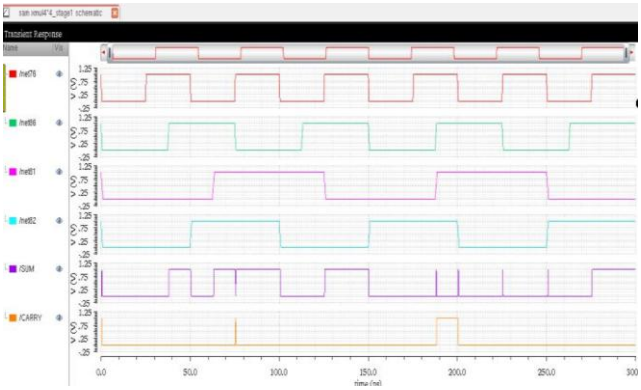

Fig. 8 Multiplier cell simulation results

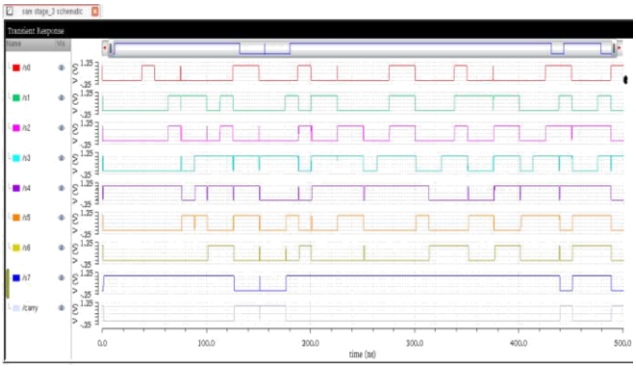

Fig. 9 Final Multiplier simulation results

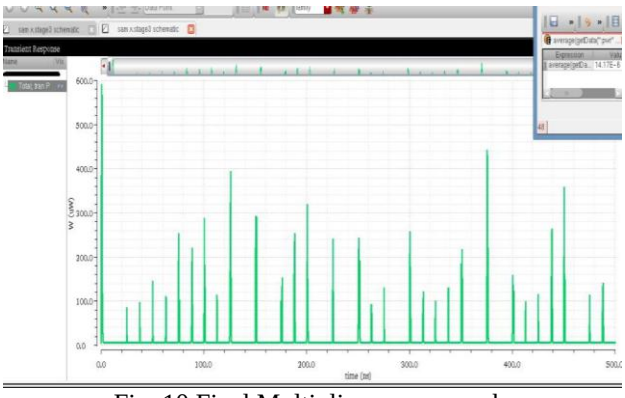

Fig. 10 Final Multiplier power graph

All the simulation results are shown in graphs with voltage depicted on Y-axis and time depicted on X-axis. For the power graph, which is shown as Fig 10, the X-axis is time and Y-axis is watts.

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V. MATHEMATICAL ANALYSIS FOR SYSTOLIC ARRAY MULTIPLIER OF REVERSIBLE LOGIC

5.1 Number of Gates (NOG)

Number of gates is calculated by counting all the gates used in individual cells. To design Systolic Array Multiplier with Reversible Logic circuit, Four MC cells, Twelve PFA gates and Nine TG gates are used. In designing Peres Full Adder gate, two cascaded peres gates are used. So, to calculate total number of gates, the expression is given as follows

$$NOG_{SYS} = NOG_{MC} + NOG_{PFA} + NOG_{TG}$$
$$= 4[2(TG) + 1(PFA)] + 12(PFA) + 9(TG)$$
$$= 33 \quad (1)$$

5.2. Garbage output calculation (GO)

The total Garbage Output for the proposed Systolic Array Multiplier with Reversible Logic circuit is given by the following expression

$$GO_{SYS} = GO_{MC} + GO_{PFA} + GO_{TG}$$
$$= 4\times6 + 12\times2 + 9\times2$$
$$= 66 \quad (2)$$

5.3 Calculating Quantum cost

The quantum cost for the proposed Systolic Array Multiplier with Reversible Logic is

$$QC_{SYS} = QC_{MC} + QC_{PFA} + QC_{TG}$$
$$= 4[2(QC_{TG}) + 1(QC_{PFA})] + 12(QC_{PFA}) + 9(QC_{TG})$$
$$= 4[2*(5) + 1(8)] + 12(8) + 9(5)$$
$$= 213 \quad (3)$$

5.4. Power calculation

The total power for proposed systolic array multiplier circuit using reversible logic is given by the following expression

$$P_{SYS} = P_{MC} + P_{PFA} + P_{TG}$$

The power of individual cells is given below.

PMC= 1.478 W PPFA= 1.169 W PTG= 499.4nW

$$P_{SYS} = 1.478\ W + 1.169\ W + 499.4nW$$
$$= 3.146\ W \quad (4)$$

VI. CONCLUSION

This paper provides unprecedented approach to reduce power consumption in irreversible Systolic Array Multiplier using reversible logic gates. Proposed reversible Systolic Array Multiplier circuit has 33 logic gates and overall power consumption is 14.7 W. Garbage output is 66 and quantum cost is 213. Simulations of the proposed designs are implemented with cadence virtuoso 90nm CMOS technology.

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